2. (amended) A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,

A2

wherein

a) the data are read from a memory organized on a page-for-page basis,

b) the data are stored in a buffer memory,

c) the intermediate step prescribed by the transform is carried out, and

d) the resulting data are written page-for-page from the buffer memory to the memory organized on a page-for-page basis.

3. (amended) A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,

A3

wherein

the data are read from two memories organized on a page-for-page basis, such that the reading is organized on a page-for-page basis, the intermediate step prescribed by the transform is carried out, and

the resulting data are again written page-for-page to the two memories organized on a page-for-page basis.

4. (amended) The method as claimed in claim 1, wherein the discrete orthogonal transform is formed by an FFT, IFFT, DCT or IDCT.

7. (amended) An apparatus for carrying out the method as claimed in claim 1 wherein

the apparatus has a memory organized on a page-for-page basis, a processor and a directly organized memory which is arranged downstream of the processor.

8. (amended) An apparatus for carrying out the method as claimed in claim 1 wherein

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the apparatus has a memory organized on a page-for-page basis, a processor and a directly organized memory which is arranged upstream of the processor.

9. (amended) The apparatus as claimed in claim 7, wherein the page-oriented memory is a large memory in relation to the directly organized buffer memory.

10. (amended) The apparatus as claimed in claim 9, wherein a fast memory is used for the buffer memory.

11. (amended) The apparatus as claimed in claim 7, wherein the page-oriented memory is a dram and buffer memory is an SRAM.

12. (amended) The apparatus as claimed in claim 7, wherein the page-oriented memory has a size of 8 K addresses and the buffer memory has a size of 32 - 64 addresses.

13. (amended) An apparatus for carrying out the method as claimed in claim 3 wherein

the apparatus has two memories organized on a page-for-page basis and a processor.

14. (amended) The apparatus as claimed in claim 13, wherein the page-oriented memories are of the same size.

A4

15. (amended) The apparatus as claim in claim 14, wherein the page-oriented memory has a size of 4 K addresses.

16. (amended) The apparatus as claimed in claim 7, wherein the processor provides a Butterfly.

IN THE SPECIFICATION:

Please add the attached Abstract to the specification.

Respectfully submitted,

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